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METHOD AND APPARATUS FOR USING A

CAPACITOR ARRAY TO MEASURE

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ALIGNMENT BETWEEN SYSTEM

COMPONENTS

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GOVERNMENT LICENSE RIGHTS

Related Application

[0002] This application hereby claims priority under 35 U.S.C. §119 to U.S. Provisional Patent Application No. 60/505,105, filed on 22 September 2003,

25 entitled "Capacitor Array and Circuit to Measure Six Degrees of Alignment," by inventors Robert J. Drost, Ronald Ho and Robert Proebsting (Attorney Docket No. SUN04-0191PSP). This application is also a continuation-in-part of, and hereby claims priority under 35 U.S.C. § 120 to, U.S. Patent Application Serial

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No. 10/741,961, entitled, "Method and Apparatus for Aligning Semiconductor Chips Using an Actively Driven Vernier," by inventors Robert J. Drost and Ivan E. Sutherland filed on 19 December 2003 (Attorney Docket No. SUN-P9704-SPL).

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BACKGROUND

Field of the Invention

[0003] The present invention relates to mechanisms for precisely aligning
10   system components, such as semiconductor chips. More specifically, the present invention relates to a method and an apparatus that uses a capacitor array to measure alignment between system components.

Related Art

15   [0004] Advances in semiconductor technology presently make it possible to integrate large-scale systems, including tens of millions of transistors, into a single semiconductor chip. Integrating such large-scale systems onto a single semiconductor chip increases the speed at which such systems can operate, because signals between system components do not have to cross chip boundaries,
20   and are not subject to lengthy chip-to-chip propagation delays. Moreover, integrating large-scale systems onto a single semiconductor chip significantly reduces production costs, because fewer semiconductor chips are required to perform a given computational task.

[0005] Unfortunately, these advances in semiconductor technology have
25   not been matched by corresponding advances in inter-chip communication technology. Semiconductor chips are typically integrated onto a printed circuit board that contains multiple layers of signal lines for inter-chip communication.

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However, signal lines on a semiconductor chip are about 100 times more densely packed than signal lines on a printed circuit board. Consequently, only a tiny fraction of the signal lines on a semiconductor chip can be routed across the printed circuit board to other chips. This problem creates a bottleneck that

5   continues to grow as semiconductor integration densities continue to increase.

[0006] Researchers have begun to investigate alternative techniques for communicating between semiconductor chips. One promising technique involves integrating arrays of capacitive transmitter plates and receiver plates onto semiconductor chips to facilitate inter-chip communication. If a first chip is

10 situated face-to-face with a second chip so that transmitter plates on the first chip are capacitively coupled with receiver plates on the second chip, it becomes possible to transmit signals directly from the first chip to the second chip without having to route the signal through intervening signal lines within a printed circuit board. Other possible chip-to-chip communication techniques involve using

15 optical fibers to couple light energy between chips, or using wire loops to couple magnetic fields between chips.

[0007] However, it is not a simple matter to align semiconductor chips with sufficient accuracy to facilitate chip-to chip communication. Conductive plates must align to couple electric fields. Optical fibers must align to couple

20 light energy. Wire loops must align to couple magnetic fields. This alignment process must be extremely precise because these conductive plates, optical fibers and wire loops are generally a small fraction of the size of a semiconductor die, and in some cases can approach the smallest possible feature size that can be manufactured on a semiconductor substrate.

25 [0008] Hence, what is needed is a method and an apparatus for aligning semiconductor chips with sufficient accuracy to facilitate inter-chip communication.

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SUMMARY

[0009] One embodiment of the present invention provides a system that measures alignment between a first semiconductor die and a second semiconductor die. The system operates by applying a pattern of voltage signals to a two-dimensional array of conductive transmitter elements that form a transmitter array on the first semiconductor die. This transmitter array is positioned over a corresponding two-dimensional array of conductive receiver elements that form a receiver array on the second semiconductor die, whereby a voltage signal applied to a transmitter element induces a voltage signal in one or more receiver elements. The system amplifies voltage signals induced in receiver elements in the receiver array, and subsequently analyzes the amplified signals to determine an alignment between the first semiconductor die and the second semiconductor die.

[0010] In a variation on this embodiment, transmitter elements have a different spacing than receiver elements, whereby a two-dimensional vernier alignment structure is created when the transmitter array is located over the receiver array.

[0011] In a variation on this embodiment, the transmitter array is organized as a two-dimensional $n \times m$ grid including nm conductive elements, and the receiver array includes at least three conductive elements which are not collinear.

[0012] In a variation on this embodiment, the receiver array is organized as a two-dimensional $n \times m$ grid including nm conductive elements, and the transmitter array includes at least three conductive elements which are not collinear.

[0013] In a variation on this embodiment, the system determines six degrees of alignment, including: an x alignment parallel to plane of the receiver

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array; a y alignment parallel to plane of the receiver array and normal to the x axis; a z alignment normal to the plane of the receiver array; an angular alignment, θ, about the z axis; an angular alignment, Ψ, about the y axis; and an angular alignment, Φ, about the x axis.

[0014] In a variation on this embodiment, the system analyzes coupling capacitances between individual receiver elements and individual transmitter elements to determine the x alignment, the y alignment and the angular alignment, θ.

[0015] In a variation on this embodiment, the system analyzes the coupling capacitances by determining a nearest neighbor mapping between receiver elements and transmitter elements.

[0016] In a variation on this embodiment, the system uses a mapping function generated by a three-dimensional capacitance field solver simulation to determine the z alignment, the angular alignment, Ψ, and the angular alignment, Φ.

[0017] In a variation on this embodiment, the system determines the z alignment, the angular alignment, Ψ, and the angular alignment, Φ, by summing capacitances between individual receiver elements in the receiver array and all transmitter elements in the transmitter array, thereby effectively considering the transmitter array to be one large plate.

[0018] In a variation on this embodiment, the system determines the z alignment, the angular alignment, Ψ, and the angular alignment, Φ, by summing capacitances between individual transmitter elements in the transmitter array and all receiver elements in the receiver array, thereby effectively considering the receiver array to be one large plate.

[0019] In a variation on this embodiment, the system is configured to electrically vary the pitch of the transmitter array by grouping together adjacent transmitter elements.

[0020] In a variation on this embodiment, the system is configured to electrically vary the pitch of the receiver array by grouping together adjacent receiver elements.

[0021] In a variation on this embodiment, transmitter elements and receiver elements can be: square, rectangular, hexagonal, triangular, oval, or round.

[0022] In a variation on this embodiment, transmitter elements are located in a metal layer of the first semiconductor die and are not covered by higher layers of metal, and receiver elements are located in a metal layer of the second semiconductor die and are not covered by higher layers of metal.

BRIEF DESCRIPTION OF THE FIGURES

[0023] FIG. 1A illustrates how a capacitor array is used to measure alignment between two parts in accordance with an embodiment of the present invention.

[0024] FIG. 1B presents a flow chart illustrating the process of measuring alignment between two parts in accordance with an embodiment of the present invention.

[0025] FIG. 2 illustrates six degrees of alignment in accordance with an embodiment of the present invention.

[0026] FIG. 3 illustrates a section of a capacitor array in accordance with an embodiment of the present invention.

[0027] FIG. 4 illustrates mutual capacitance between transmitter and receiver plates in accordance with an embodiment of the present invention.

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[0028] FIG. 5 illustrates a two-dimensional vernier pattern in accordance with an embodiment of the present invention.

[0029] FIG. 6 illustrates a nearest neighbor mapping in accordance with an embodiment of the present invention.

[0030] FIG. 7 illustrates a nearest neighbor mapping for translation misalignment in the x direction in accordance with an embodiment of the present invention.

[0031] FIG. 8 illustrates a nearest neighbor mapping for rotational misalignment in accordance with an embodiment of the present invention.

[0032] FIG. 9A illustrates a triangular plate arrangement in accordance with an embodiment of the present invention.

[0033] FIG. 9B illustrates another triangular plate arrangement in accordance with an embodiment of the present invention.

[0034] FIG. 9C illustrates a hexagonal plate arrangement in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0035] The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

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Alignment Mechanism

[0036] One embodiment of the present invention includes alignment structures located on two separate parts, wherein the alignment structures facilitate a relative position measurement between the parts. In one embodiment of the present invention, each part is a separate semiconductor chip, and the alignment structures facilitate alignment of the semiconductor chips to facilitate communication between the semiconductor chips.

[0037] The alignment structure on each part includes a planar region with metal plates that form one side of a capacitor array. When the two parts are brought into close proximity to each other, mutual capacitive coupling between plates in the two structures can be measured using the known capacitance measurement techniques. (For example, see U.S. Patent No. 5,212,454, "Method and Apparatus for Selecting and Measuring a Capacitance from a Plurality of Interconnected Capacitances," by inventor Robert J. Proebsting.) By analyzing these mutual capacitance measurements, six degrees of alignment between the two structures can determined as is described in more detail below with reference to FIGs. 1A-9C.

[0038] More specifically, FIG. 1A illustrates parts A and B. Part A includes a planar region (indicated by a thick rectangle) that contains one side of a capacitor array structure. Note that for part A the capacitor array structure faces into the page. Similarly, part B includes a planar region (indicated by a thick rectangle) that contains the other side of the capacitor array structure. Note that for part B the capacitor array structure faces out of the page. In this way, when parts A and B are placed together the two sides of the capacitor array structure are in close proximity to each other. It is then possible to perform capacitance measurements between the capacitor arrays found on parts A and B to determine six degrees of alignment between parts A and B.

[0039] FIG. 1B presents a flow chart illustrating the process of measuring alignment between two parts A and B in accordance with an embodiment of the present invention. The process starts by applying a pattern of voltage signals to the two-dimensional transmitter array (step 102). This pattern of voltage signals

5   induces corresponding voltage signals in conductive elements in the two-dimensional receiver array through capacitive coupling (step 104). These induced signals are amplified (step 106) and the amplified signals are subsequently analyzed (step 108) to determine the alignment between parts A and B.

10   **Six Degrees of Alignment**

[0040] FIG. 2 illustrates six degrees of alignment between parts A and B. In one embodiment of the present invention, capacitance measurements and subsequent analysis allows x, y and θ alignments to be measured in absolute coordinates. The z, Ψ, and Φ alignments can be relatively measured and

15   correlated to absolute values by using a mapping function generated by a three-dimensional capacitance field solver simulation.

Capacitor Array

[0041] FIG. 3 illustrates an exemplary section of a capacitor array. Note

20   that one instance of this capacitor array is located on the transmitter and another instance is located on the receiver. The plates are labeled $P_{i,j}$, wherein the subscripts i and j specify their position in the array.

[0042] Parameters for the transmitter and receiver arrays may differ. For example, the x-pitch, dx, and/or the y-pitch, dy, may be different, or the total

25   number of rows or columns may be different. Furthermore, the elements in the arrays can be squares, as shown, or can be other shapes such as rectangles, triangles, hexagons, circles or ovals. Note that if the transmitter and receiver

arrays are located on integrated circuits, the elements of the arrays can be plates in a topmost metal layer, or in a lower metal layer that is not covered by higher metal layers.

[0043] FIG. 4 presents a cross-sectional view of some transmitter and receiver plates. In this cross-sectional view, Pt refers to the transmitter plates, and Pr refers to the receiver plates. Note that the transmitter and receiver plates are misaligned by distance $x1$. As a result, some of the capacitance that was intended to couple between $Pt_{i,j}$ and $Pr_{i,j}$, illustrated as capacitor C_b, instead couples to $Pr_{i-1,j}$, illustrated as capacitor C_a. The relative size of C_b and C_a provides information about the misalignment distance $x1$. If $x1$ is less than half of the transmitter plate pitch, then C_b will exceed C_a. If $x1$ is more than half of the transmitter plate pitch, then C_b will exceed C_a. These capacitances can be measured using the capacitance measurement circuit and method described in U.S. Patent No. 5,212,454.

[0044] By comparing the coupling capacitance from one receiver plate to each of the transmitter plates we can determine which transmitter plate is closest to the receiver plate. We call this closest transmitter plate the "nearest neighbor" to the receiver plate. Note that most transmitter plates have almost no coupling to most of the receiver plates. Only the transmitter plates that have some overlap area or fringe field coupling to a receiver plate will have a measurable capacitance. We can repeat this measurement for each receiver plate to obtain a mapping from all of the receiver plates to their nearest neighbors.

Two-Dimensional Vernier Pattern

[0045] FIG. 5 illustrates a two-dimensional Vernier pattern for a 7 by 7 array of receiver plates under a 8 by 8 array of transmitter plates. (The transmitter plates are shaded and the receiver plates are not.) Note that the transmitter and

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receiver plates have different pitches so that they form a two-dimensional Vernier pattern, which can be used to accurately measure both x and y offsets.

Nearest Neighbor Mapping

5   [0046] FIG. 6 illustrates both transmitter and receiver plate arrays as well as arrows indicating a nearest neighbor mapping that would be made after the capacitance is measured. (The transmitter plates are shaded and the receiver plates are not.) For some receiver plates, the arrow points in a diagonal direction, indicating that the receiver plate is closest to a single diagonally offset transmitter

10   plate. Note that the receiver plates in the middle column and row have two nearest neighbors because the capacitances to two transmitter plates are equal. For these receivers, the arrows point horizontally or vertically. For the center receiver plate, the capacitances to four transmitter plates are equal. Hence, no arrow is shown.

15   [0047] FIG. 7 similarly illustrates transmitter and receiver plate arrays along with arrows indicating a nearest neighbor mapping, except that the receiver plates are shifted in the x direction. (The transmitter plates are shaded and the receiver plates are not.) Note that in FIG. 7 the nearest neighbors have changed from FIG. 6. Furthermore, note by examining these changes it is possible to

20   determine the magnitude of the misalignment.

Rotational Alignment

[0048] FIG. 8 similarly illustrates a nearest neighbor mapping, except that the receiver plate array is rotated by five degrees relative to the transmitter plate

25   array. Again, the mapping changes as a function of the misalignment between the transmitter and receiver arrays.

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[0049] For z-measurements and tilts in Ψ and Φ between the plate arrays we can sum the capacitance measurements between a single receiver plate and all transmitter plates rather than measuring individual mutual capacitance between transmitter and receiver plates. This summation can be performed after individual plate to plate mutual capacitances are measured, or alternatively, a number of transmitter plates can be connected together during the analog capacitance measurement so that one measurement measures the total capacitance. (Alternatively, note that we can similarly sum capacitance measurements between a single transmitter plate and all receiver plates.)

[0050] Summing capacitances between the receiver plate and all the transmitter plates (or, alternatively between the transmitter plate and all the receiver plates) causes the transmitter plates to act as one large plate. In this mode, x or y shifts and θ rotations have little effect on the measured capacitance because a plane of small tightly-packed plates acts similarly to a solid plane in terms of capacitive coupling.

[0051] For the z distance, and Ψ and Φ tilt measurements, the measured capacitances can be correlated to distance or tilt through a mapping function created using a three-dimensional field solver. For each receiver plate, we can correlate the capacitance to a distance. Across the entire array of receiver plates, the average z-distance can be used as the distance between the receiver and transmitter plate arrays. The tilts in Ψ and Φ can be determined based on the change or slope in the z distance as a function of x and y position.

Variations

[0052] Note that pitch can be varied along x and y dimensions if alignment is more critical in one dimension. Pitch can also be electrically varied by grouping together sets of transmitter or receiver plates. For faster testing, groups

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of transmitter plates and receiver plates can be ganged together, for example in a 2 by 2 or a 4 by 4 arrangement. In this case, measurements will take fewer steps but will be less accurate. Furthermore, plates can be shapes other than rectangles. For instance, the transmitter and receiver arrays could be arrays of triangles or hexagons as are illustrated in FIGs. 9A-9C.

[0053] We can also connect transmitter plates into vertical bars for x measurements, and into horizontal bars for y measurements. Two or more measurement arrays can be separated by some distance in order to increase the sensitivity in measuring θ, Ψ, or Φ misalignments. For these misalignments measurements, increasing the maximum span of the measurement structure improves the measurement sensitivity.

[0054] Plates in the array can also have two or more physical pitches. This can provide variable resolution to the measurement, thereby easing initial alignment using a large pitch, but improving final alignment accuracy using a fine pitch.

[0055] Also note that it is not necessary to use a complete n by m array of transmitter plates and a complete n by m array of receiver plates. In fact, if an n by m array of transmitter plates is used, it is possible to determine six degrees of alignment using only three receiver plates, as long as the receiver plates are not colinear. Similarly if an n by m array of receiver plates is used, it is possible to determine six degrees of alignment using only three transmitter plates, as long as the transmitter plates are not colinear.

[0056] The foregoing descriptions of embodiments of the present invention have been presented only for purposes of illustration and description. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not

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intended to limit the present invention. The scope of the present invention is defined by the appended claims.